Abstract of the Disclosure

A high performance audio processing device having significantly increased reconfigurability capabilities and that offers far more precision and throughput than its predecessors without increasing the per-channel cost of the device above the per-channel cost of the predecessors. The device architecture includes a single-cycle, 48X28 bit multiply feature that is configured as a sophisticated switch to minimize the use of branching such that the reconfiguration capabilities of the device are significantly increased. Multiplying by zero shuts a path off, while multiplying by one turns the path on, and multiplying by –1 turns the path on, but with an inversion of the path signal's phase. The use of a full-precision multiply rather than other forms of decision logic also allows "morphing" from one setting to another on-the-fly, and provides new operating states that are linear combinations of the "on" and "off" settings.